SGS-THOMSON MICROELECTRONICS

ISB28000 SERIES

HCMOS EMBEDDED ARRAY

PRELIMINARY DATA

FEATURES

- Combines Standard Cell features with Sea Of Gates time to market.
- 0.7 micron triple layer metal HCMOS process featuring self-aligned twin tub N and P wells, low resistance polysilicide gates and thin metal oxide.
- 2 - input NAND (ND2P) delay of 0.25 ns (typ) with fanout = 2
- 5 V, 3.3 V and mixed voltage library versions.
- Embedded functions for High Density SPRAM, DPRAM, ROM and FIFO.
- Video DAC (3 x 8 Bit) for graphics applications at 80 or 135 MHz.
- Phase Locked Loop function for chip to chip clock management and frequency synthesis.
- Metallised functions to support SPRAM, DPRAM and ROM.
- Fully independent power and ground configurations for core and I/O cells.
- Variable I/O ring capability from 48 to 400 pads.
- Output buffers capable of driving ISA, EISA, MCA, and SCSI interface levels.
- True not pseudo TTL interface
- High drive I/O capability of sinking up to 24 mA (48 mA option)with slew rate control and current spike suppression.
- Active pull up and pull down devices.
- Buskeeper I/O functions.
- Oscillators for wide frequency spectrum.
- Broad range of 228 SSI and core cells.
- 200 element macrofunction library
- Design For Test includes LSSD macro library option for megacells and IEEE 1149.1 JTAG Boundary Scan architecture.
- Cadence based design system with interfaces from multiple workstations.
- Broad ceramic and plastic package range
- Latchup trigger current > +/- 200 mA.
- ESD protection > +/- 2000 volts

EMBEDDED FUNCTIONS

MEGACELLS				MEGAFUNCTIONS		
SPRAM-E	**DPRAM**	**ROM**	**FIFO-E**	**VIDEODAC**	**FREQ SYNTHESIS PLL**	**CLOCK MULTIPLIER PLL**
80 Kbit max capacity	64 Kbit max capacity	64 Kbit max capacity	64 Kbit max capacity	Triple DAC with 8 bit resolution	Input Freq. 1 - 4 MHz	Input Freq. 4 MHz
8 to 16 K W -1 to 80 bit	16 to 8 K W - 1 to 80 bit	32 to 8 K W - 1 to 32 bit	16 to 8 K W - 1 to 80 bit	Comparators on outputs	Output Freq 6 to 32 MHz	Output Freq. 16.25 to 136 MHz
Access Time (1k x 16b) 4.5 ns Typ.	Access Time (1k x 16b) 15 ns Typ.	Access Time (1k x 8b) 7 ns Typ.	Access Time (2k x 8b) 12 ns Typ.	135 MHz operation	Jitter Error + / - 0.5 ns	Jitter Error + / - 1 ns
Density 27 kbit/mm^2 (1k x 16b)	Density 1.9 kbit/mm^2 (1k x 16b)	Density 12 kbit/mm^2 (1k x 8b)	Density 1.6 kbit/mm^2 (2k x 8b)			

GENERAL DESCRIPTION

The ISB28000 EMBEDDED™ ARRAY series uses a high performance, triple level metal HCMOS process to achieve sub-nanosecond internal speeds, while at the same time, offering low power dissipation and high noise margin. The die size is variable up to 216,000 wireable 2-input NAND gates. Even higher effective utilizations are achieved with the optimization of metallised and embeddable memory megacells.

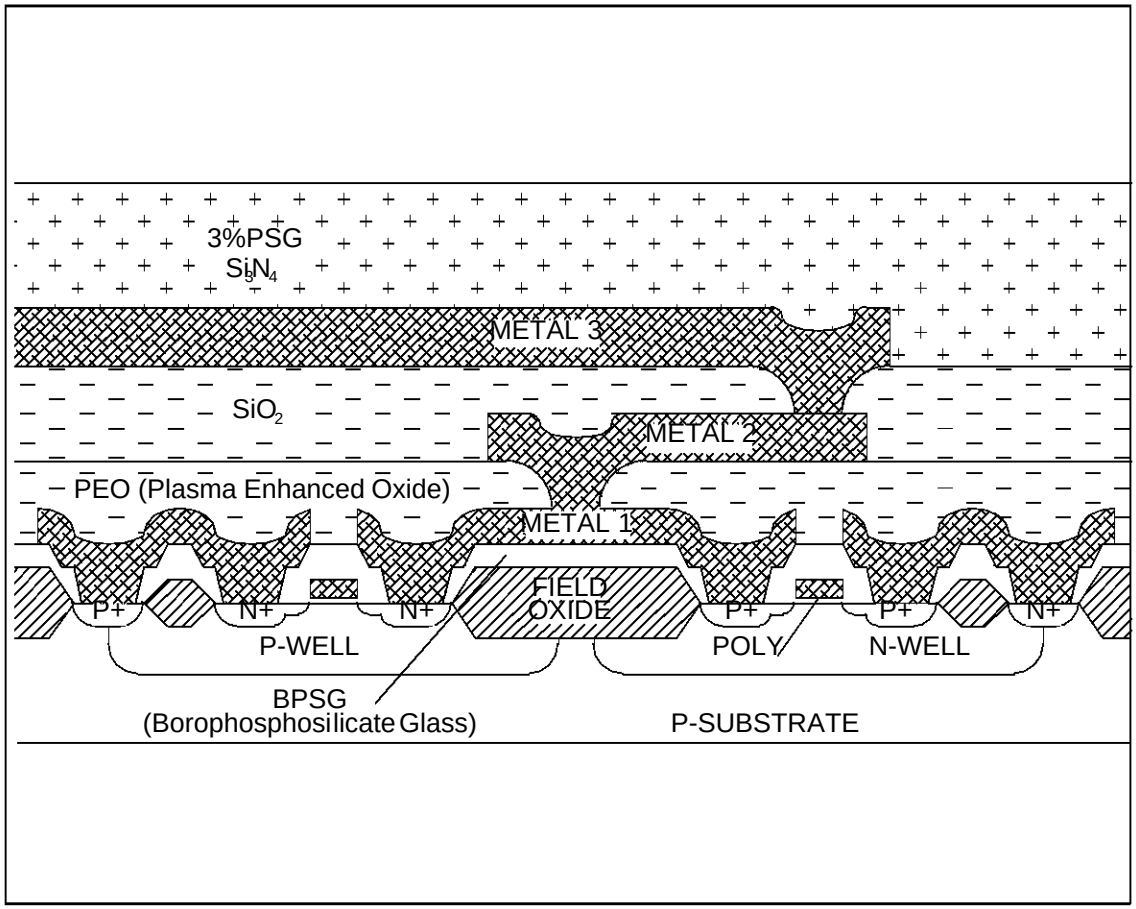
The high current I/O cell counts range from 48 to 400 full function cells. The output buffers have drive strengths capable of sinking up to 48 mA and sourcing up to 12 mA without limiting the functionality of adjoining cells. Output buffers are electrically compatible with EISA, ISA, MCA and SCSI interface standards.

The ISB28000 library is available in all 5V, all 3.3 V and a combined mixed voltage versions This allows the core and I/O to be powered from different voltage levels for an optimal combination of performance, power consumption and interface compatibility.

Testability is supported at device level with the close coupling of the scan path flip flops, automatic test pattern generation and high pattern depth tester architectures. At the system level testability, IEEE 1149.1 JTAG is fully supported.

A wide range of CAD tools are combined into the design system allowing design development on a choice of workstations. An extensive package offering makes this series well suited for a broad range of high performance applications. The product technology may be used in commercial, industrial and military environments.

Figure 1. Triple Level Metal Architecture



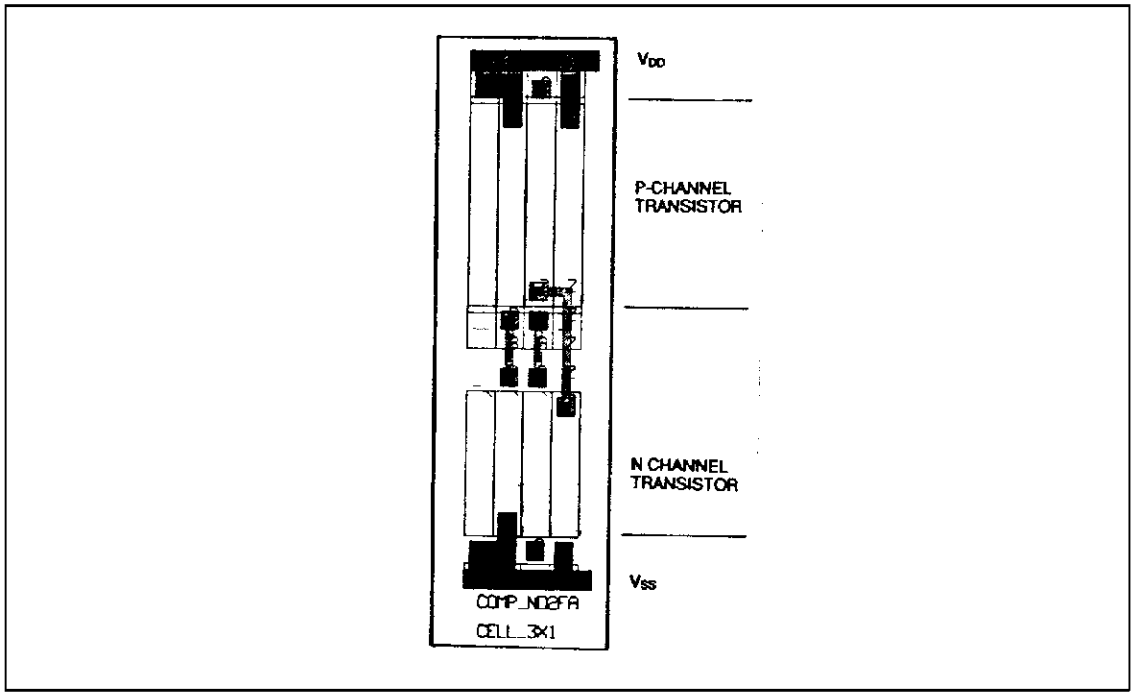
TECHNOLOGY OVERVIEW

The ISB28000 Series Embedded Array is an evolution of the CONTINUOUS ARRAY™ architecture with the added capability of embedded functions for the core and periphery. The embedded functions can be used for high density RAMs where performance is the prime criteria. The core is amatrix of potentially active transistors. Surrounding the core are the configurable I/O cells,and V_{DD} / V_{SS} pads occupying pre-established locations. Three levels of metal are used as shown in Figure 1. Intracell and intercell wiring are limited to first level metal with the second and third metal levels dedicated to interconnect wiring and power distribution. The reduced geometry of the ISB28000 transistors can only be used to full advantage with short interconnect between macrocells. The third level of metal greatly reduces the interconnect and increases the gate utilization to an average 75%. Further advantages include improved power dissipation and increased performance.

The basic cell is a pair of N and P channel transistors that are vertically arranged. The width of the P channel transistor is larger than the N channel transistor thereby providing improved symmetry between the rise and fall times of macrocells. The basic cells are placed adjacent to each other without field isolation to form a multiple column row. Adjacent basic cells may be uniquely wired together to form a variety of macrocells. Isolation between macrocells is accomplished by placing the endmost basic cell in the cutoff state, thus providing flexibility and space efficiency. Each basic cell has 17 horizontal wiring channels on first metal,1 vertical wiring channel on second metal and 15 horizontal wiring channels on third metal.

As can be seen from Figure 2, the first metal V_{DD} and V_{SS} power lines run horizontally on the top and bottom of each row. Every other row is flipped relative to the previous row thereby allowing the sharing of supply lines between adjacent rows. Additionally, a 2 column wide vertical power screen is provided every 36 columns on second metal.A third power screen is provided which is a replica of the first level power screen but with opposite polarity.

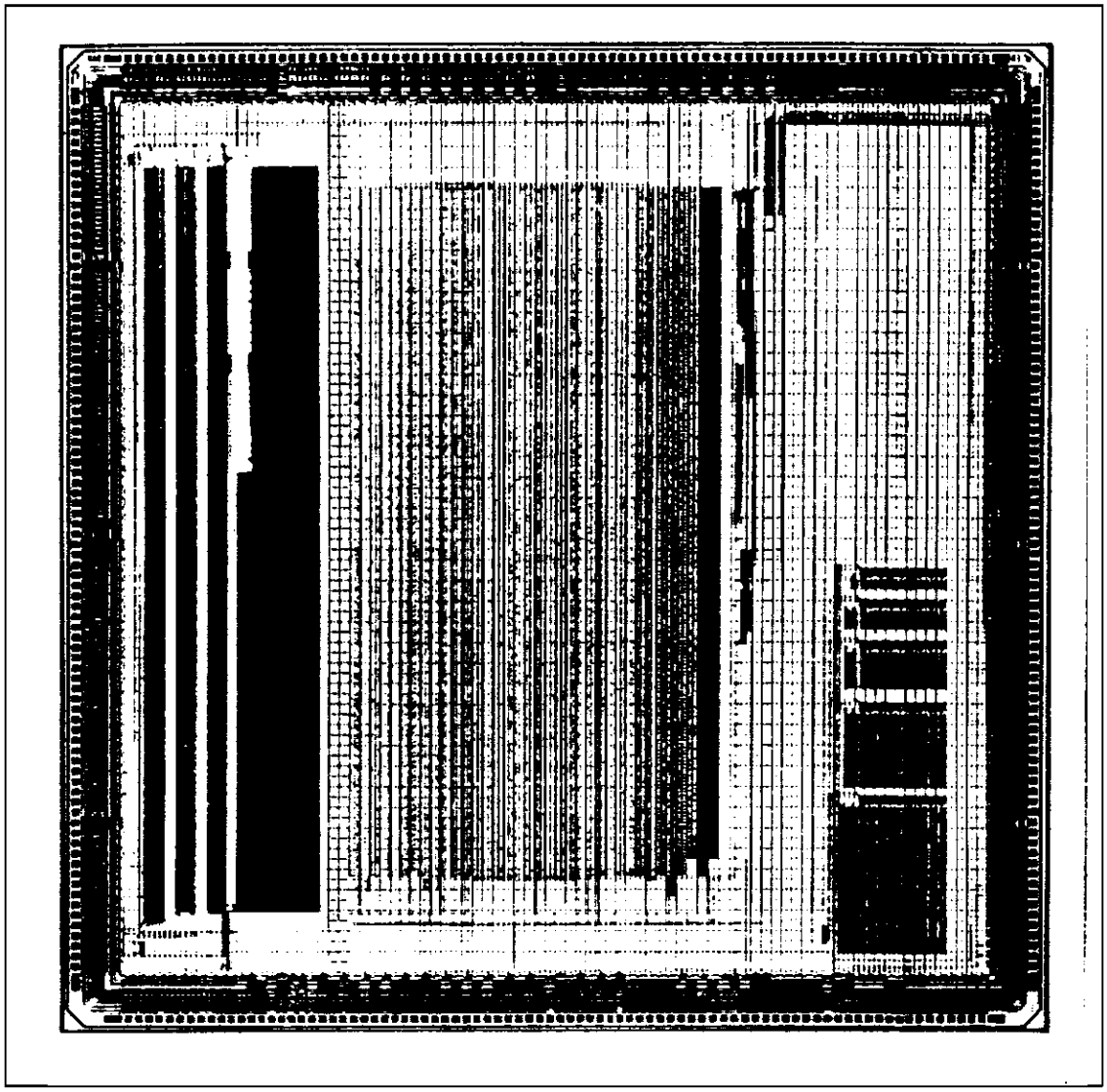
Figure 2. Internal Core Cell ND2



EVALUATION DEVICE

An evaluation device is used to demonstrate the performance of the ISB28000 series as well as verify the effecti-veness of the design system. The device has path delays, latches, a host of macrocells and embedded functions which were used to verify the simulated characteristics that are supplied in the data book.Characterization of the path delays including interconnect shows typical delays of 250 ps for a 2 input NAND with receivers/drivers operating at frequencies in excess of 100 MHz.The evaluation device is avai-lable in a 208 pin guard quad flat pack.

Figure 3. Evaluation Device



LIBRARY

The following section details the elements which make up the ISB28000 Series library. The elements are organized into three categories

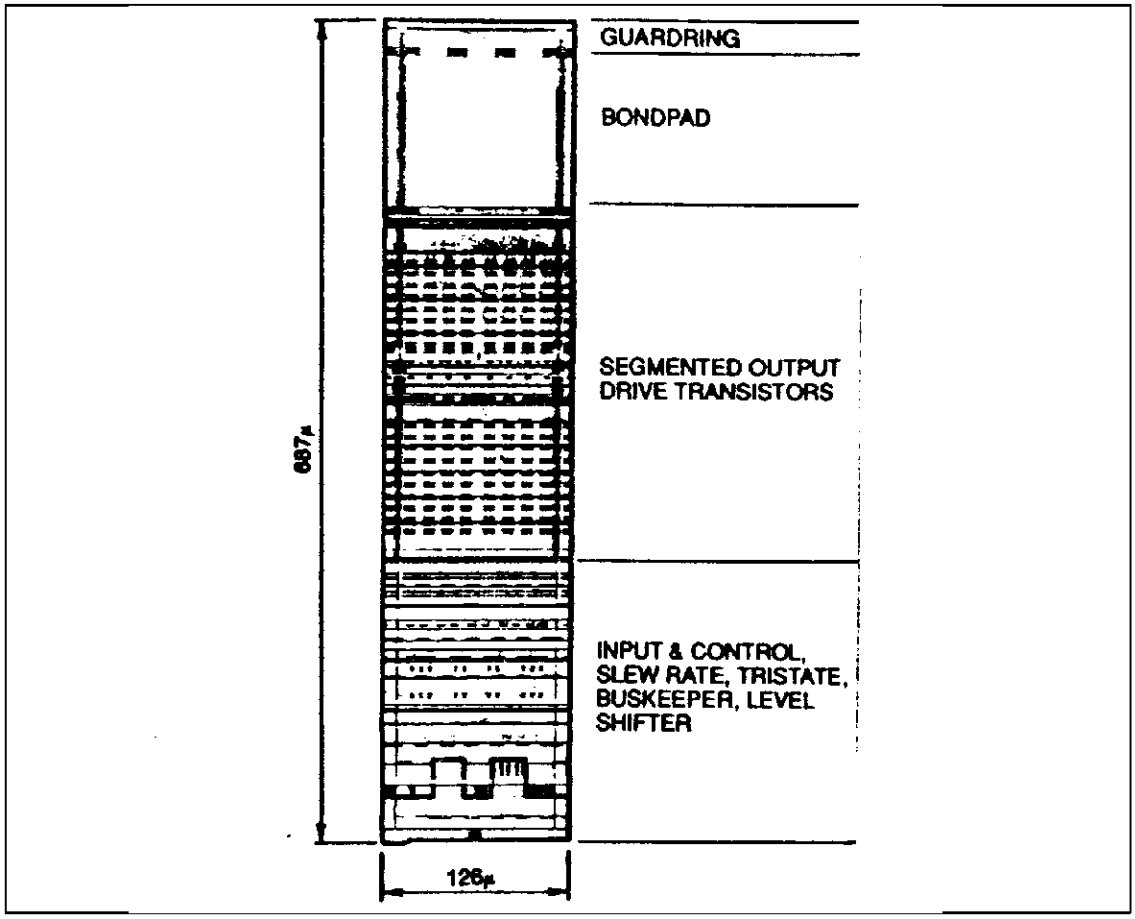
1. Macrocell libary with Input, Output, Bidirectional Buffers and Core cells including JTAG macrocells.
2. Macrofunctions
3. Module Generators
4. Embedded Functions

I/O Buffers

The I/O buffers are located on the periphery of the array. Figure 4 is a plot of an I/O buffer. The basic cell consists of a bond pad with an input protection, an output driver section and a receiver/pre-driver section. Every I/O may be configured as either input, output, bidirectional, tri-state output, tri-state bidirectional, or additional V_{DD}/V_{SS}. High impedance pull-up or pull-down resistors are also available in the I/O cell resistors. Input and output macrocells do not invert logic signals. The output transistors are provided with an independent power distribution metalization thereby minimizing switching transients in the periphery from affecting either the on chip receivers or the internal matrix.

Several important features are incorporated in the output drivers. These include slew rate control and current spike suppression. Slew rate is controlled by turning on individual sections of the large output transistor in a controlled manner. During normal switching a large surge of current occurs when a conventional CMOS buffer has both P and N channel transistors in conduction. This situation is avoided by placing the buffer in tri-state for approximately 200 ps during the time the buffer changes state. Each output buffer may be configured for up to 24 mA current drive capability.

Figure 4. Full Function I/O Cell



True TTL Compatibility. The TTL bus driver buffers are designed to operate in conjunction with bipolar products on a common data bus. The output voltage swings and current drive capabilities are the same as bipolar TTL buffers. This allows the system designer to take advantage of the low power consumption of the ISB28000 array CMOS logic while not being forced to deal with pseudo TTL buffers. Most CMOS array TTL buffers are standard CMOS buffers with new delay equations.These CMOS pseudo TTL buffers display various undesired operational nets to the 5 V rail having low impedance PMOS transistors which not only slow down the net by raising the discharge time but may also damage the bipolar TTL receivers connected to the net. The ISB28000 does not pull to rail. Another problem with pseudo TTL buffers is the high impedance input exhibited when in tri-state mode. This can cause undesired reflections on the data bus and is overcome in the ISB28000 by means of two diodes which exhibit input characteristics common to biplolar devices in tristate mode.

Standard Bus Compatibility. A subset of the TTL buffers conform to ISA, EISA, MCA and SCSI bus operating specifications. These buffers comply fully with the specification rise and fall times. Figures 5a and 5b show the D.C Specifications for True TTL Output Buffers and Input Receivers respectively.They target the high performance 32 bit RISC and CISC architectures and data communication sytems. Selection of the correct output buffer is very important to achieve the desired performance. Two parameters used to select the appropriate buffer are maximum drive current and load capacitance.

Figure 5a. D.C Specifications for True TTL Output Buffers

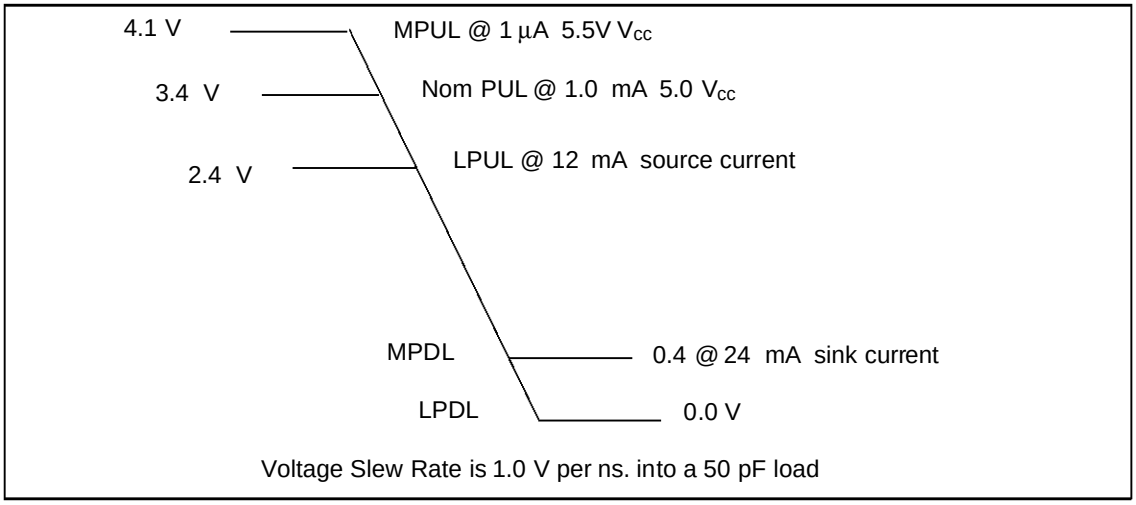
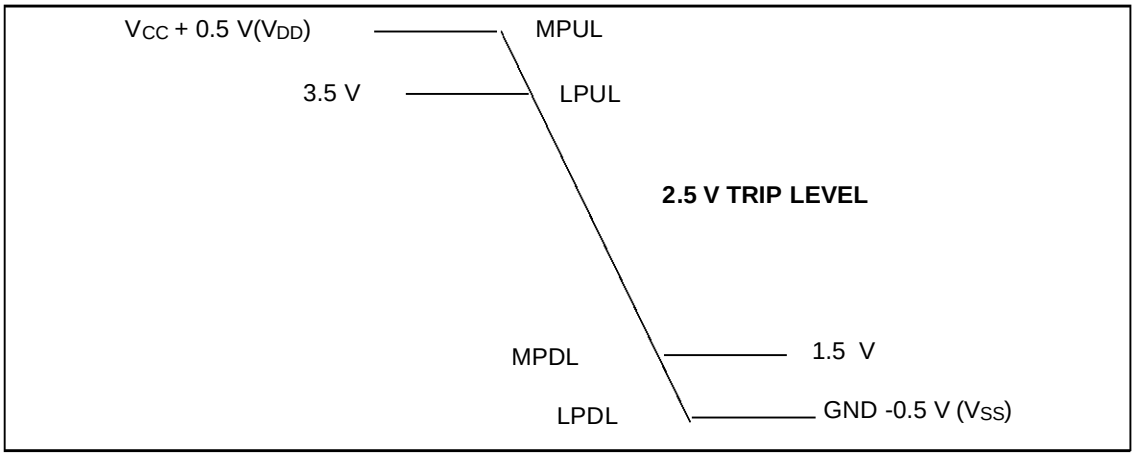


Figure 5b D.C Specifications for Input Receivers



Exceeding the maximum load capacitance will also result in slower switching performance. Exceeding the maximum current may result in degraded levels of reliability. Standard CMOS and TTL levels are specified for all external buffers. Schmitt Trigger input receivers are available. All buffers are designed for commercial, industrial and military operation.

Table 1. I/O Drive capability for slew rate control buffers

Current Drive (mA)	Standard Unit	Maximum Capacitance (pF)
4.0	0.33	100
8.0	0.67	200
12.0	1.00	300
16.0	1.33	500
24.0	2.00	750

Table 2. I/O Drive capability for non-slew rate control buffers

Current Drive (mA)	Standard Unit	Maximum Capacitance (pF)
4.0	1.0	100
8.0	2.0	200
16.0	3.0	500

Table 3. Temperature and Voltage Multipliers

Temperature (°C)	K_T
–55	0.72
–40	0.77
70	1.16
85	1.21
125	1.35
V_{DD} (V)	K_V
4.50	1.10
4.75	1.05
5.00	1.00

All pads except the eight corner pads can be configured as power or I/O pads. The configured power pads are known as placeable pads and have an associated multiplication factor dependent on the buffer drive current capability, as shown in Table 1. the current for each type of buffer is:

$$I_{Buffer} = \text{Buffer Current (max.)} \times \text{Multiply factor} \times \text{Number of Buffers}$$

Table 2 shows the Sink and Source current for typical buffers.

Core Logic

The propagation delays shown in the ISB28000 data book and in the AC Characteristics section of this data sheet are given for nominal processing, 5V operation, and 25°C temperature conditions. However there are additional factors that affect the delay characteristics of the macrocells. These include loading due to fanout and interconnect routing, voltage supply, junction temperature of the device, processing tolerance and input signal transition time. Prior to physical layout, the design system can estimate the delays associated with any critical path. The impact of the placement and routing can be back annotated from the layout for final simulations of critical timing.The effects of junction temperature, (K_T) and voltage supply, (K_V) on the delay numbers are summarized in Table 3. A third factor, is associated with process variation. This multiplier has a minimum of 0.6 and a maximum of 1.6.

Macrocells And Macrofunctions

The ISB28000 series has internal macrocells that are robust in variety and performance. Specialized cells for scan techniques and a mix of complex logic functions round off the SSI offering. High drive, double output power versions, which may be used to speed up critical paths, are available for most internal macrocells.

Macrofunctions are a series of soft-macros facilitating quick capture of large functional blocks and are available for such functions as counters, shift registers and adders. Macrofunctions are implemented at layout by utilizing macrocells and interconnecting to create the logic function.

Module Generators

A series of module generators are available to support a range of megacells. These modules enable the designer to choose individual parameters in order to create a compiled cell which meets the specific application requirements.The compiled cells are implemented using a special leaf cell technique which

Table 4. Macrocell 5V Library Summary

Function	Total
Single Drive Gates and Inverters	33
Double Drive Gates and Inverters	25
Boolean Gates	13
Internal Tristate Buffers, Single & Double Drive	4
Flip Flops, Latches and RAM1, Single Drive	15
Latches with Scan Inputs	2
Flip Flops and Latches , Single Drive	7
Flip Flops and Latches , Double Drive	11
Full Adder	1
Multiplexers, MSI, Power Multiplexers	9
CORE CELL TOTAL	**120**
Input	12
Output	34
Bidirectional	39
Buskeeper	19
I/O BUFFER TOTAL	**104**
OVERALL TOTAL	**224**

Table 5. Module Generator Library

Cell	Description
SPRAM	1 port RAM (separate dataI/O) - Synchronous - Capacity 8,192 bit max. 8 to 2K words x 1 to 64 bit (multiplex factor 1,2,4,8,16) AC Characteristics: Read access time = 6.3 ns typical (1024 Words x 8 bit)
DPRAM	2 port RAM (separate dataI/O) - Asynchronous - Capacity 4,096 bit max. 1 to 1K words x 1 to 64 bit (multiplex factor 1,2,4,8,16) AC Characteristics: Read access time = 11 ns typical (512 Words x 8 bit)
ROM	Synchronous - Capacity 16,384 bit max. 32 to 2K words x 1 to 32 bit) AC Characteristics: Read access time = 4 ns typical (512 Words x 8 bit)

ensures predictable layout and accurate module characteristics.

Generators are available for megacells such as single port RAM, dual port RAM and ROM. In choosing megacells the designer can consider the trade-offs between speed and area to generate a fully customized cell which meets their specific device requirements.

EMBEDDED FUNCTIONS

Embedded function are available for high density, high performance SPRAM, DPRAM, ROM and FIFO. These are complimented by a group of embedded megafunctions which initially consist of a Triple 8-bit DAC, Graphics RAM, Clock Multiplier PLL and Frequency Synthesis PLL.

DESIGN FOR TESTABILITY

The time and cost for ASIC testing increases exponentially as the complexity and size of the ASIC grows. Using a design for testability methodology allows large, more complex ASICs to be efficiently and economically tested.

ISB28000 supports the JTAG boundary Scan and edge level sensitive design scan by providing the necessary macrocells.Scan testing aids device testability by permitting access to internal nodes without requiring a separate external connection for each node accessed. Testability is assured at device level with the close coupling of LSSD latch elements, Automatic Test Pattern Generation (ATPG) and high pattern depth tester architecture. At system level, SGS-THOMSON fully supports IEEE 1149.1, within the array of each cell array member. Two types of scan cells are provided by the ISB28000 Series library. They are FDxS/FJKxS cells which are edge sensitive and LSxx cells which are truly LSSD cells.

PACKAGE AVAILABILITY

The ISB28000 Series is designed to be especially suitable for high volume surface mount applications, from 28 pin plastic leaded chip carriers (PLCC) up to 160 pin metric quad flatpacks (MQFP) with over 300 pin MQFPs in development. Pin counts for through board mounting range up to 299. For higher pin counts the range is compatible with the industry standard JEDEC and EIA-J Guardring Quad Flatpack (GQFP) with pin counts from 186 to 306.

The diversity in pin count and package style gives the designer the opportunity to find the best compromise for system size, cost and performance requirements.

All packages for the military market are hermetically sealed to meet MIL-STD-883 Method. Prototypes are developed in ceramic packages for fast turn-around evaluation.

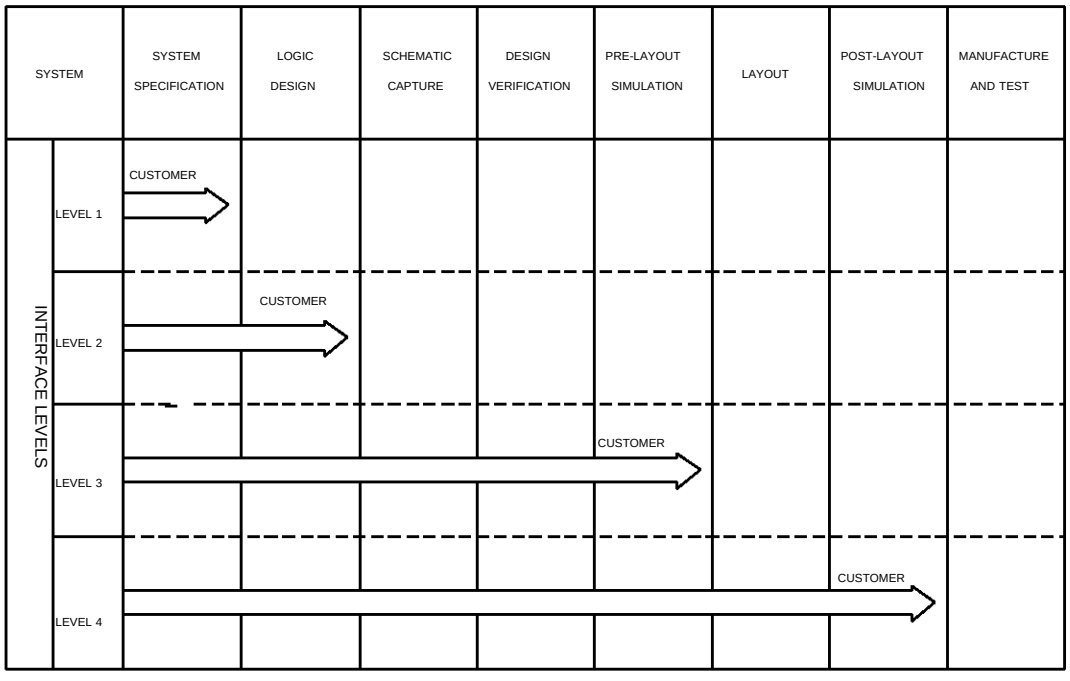
DESIGN ENVIRONMENT

Several interface levels are possible between SGS-THOMSON and the customer in the undertaking of an ASIC design. The four levels of interface are shown in Figure 6. Level 1 is characterized by SGS-THOMSON receiving the system specification and taking the design through to validation and fabrication. At Level 2 interface the designer supplies a complete logic design implemented in a standard generic logic family. SGS-THOMSON then takes the design through to layout, validation and fabrication.

Level 3 is the most common and preferred interface level. Logic capture and pre-layout simulation are performed by the designer using a SGS-THOMSON supported design kit. The design is then taken through layout, validation and fabrication by SGS-THOMSON

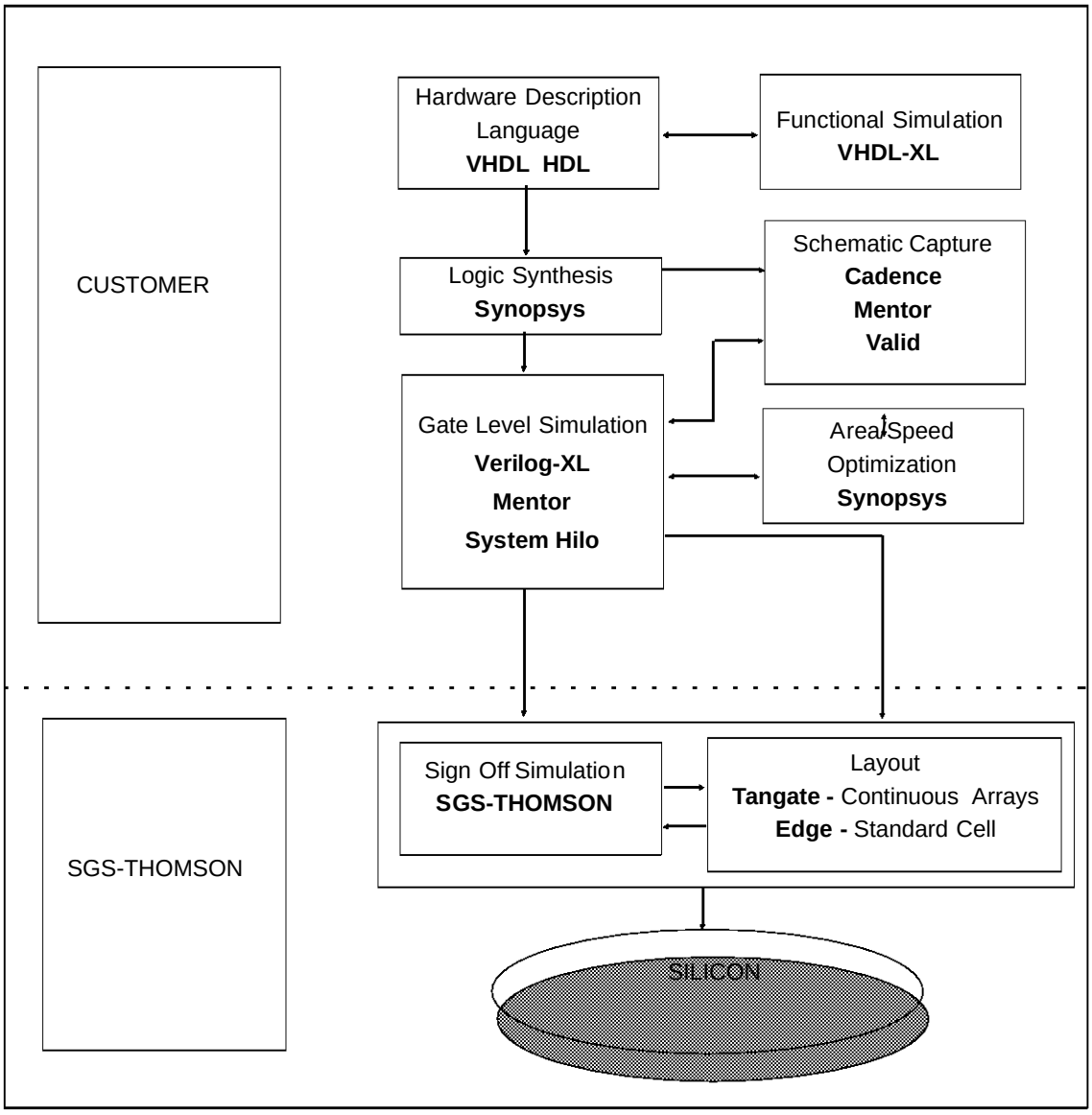
The SGS-THOMSON design system validates all designs before fabrication. Design kits are provided that allow schematic entry via Mentor Graphis, Cadence Amadeus and Valid Logic. Simula-tion is supported on Cadence Amadeus and Mentor Graphics. Full support is also provided for Cadence Verilog, VHDL-XL and System Hilo simulators. Figure 7 shows the SGS-THOMSON Design Flow.

Figure 6. Customer SGS-THOMSON Interface Levels



ISB35_VC

Figure 7. SGS-THOMSON Design-Flow



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{DD}	–0.50 V to + 7.00 V
Input or Output Voltage	–0.50 V to (V_{DD} + 0.50) V
DC Forward Bias Current, Input Or Output or Input	–12 mA (source) + 24mA (sink)
Storage Temperature (Ceramic)	–65 to 150°C
Storage Temperature (Plastic)	–40 to 125°C

Note 1: Referenced to V_{SS}. Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Operating Supply Voltage V_{DD} Commercial Industrial Military	 4.75 V to 5.25 V 4.75 V to 5.25 V 4.50 V to 5.50 V
Operating Ambient Temperature Commercial Industrial Military	 0 to + 70°C –40 to + 85°C –55 to + 125°C

DC ELECTRICAL CHARACTERISTICS Across Temperature Range (Note 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
TTL INTERFACE							
V_{IL}	Low Level Input Voltage				0.8	V	2,3
V_{IH}	High Level Input Voltage		2.0			V	2,3
V_{OL}	Low Level Output Voltage	I_{OL} = Rated buffer current		0.2	0.4	V	2,3,4
V_{OH}	High Level Output Voltage	I_{OH} = Rated buffer current	2.4	3.4		V	2,3,4
V_{T+}	Schmitt Trig. +ve Threshold			2.0	2.4	V	
V_{T-}	Schmitt Trig. –ve. Threshold		0.6	0.8		V	
CMOS INTERFACE							
V_{IL}	Low Level Input Voltage				1.5	V	3
V_{IH}	High Level Input Voltage		3.5			V	3
V_{OL}	Low Level Output Voltage	I_O =Rated buffer current			0.4	V	3,5,6
V_{OH}	High Level Output Voltage	I_O =Rated buffer current	V_{DD}–0.5			V	3,5,7
V_{T+}	Schmitt Trig. +ve Threshold			3.0	4.0	V	
V_{T-}	Schmitt Trig. –ve Threshold		1.0	1.5		V	
GENERAL							
I_{IL}	Low Level Input Current	$V_I = V_{SS}$			+1	µA	
I_{IH}	High Level Input Current	$V_I = V_{DD}$			–1	µA	
I_{OZ}	Tri-state Output Leakage	V_O = 0 V or V_{DD}			± 10	µA	
C_{IN}	Input Capacitance	Freq = 1 MHz @ 0 V		2	4	pF	8
C_O	Output Capacitance	Freq = 1 MHz @ 0 V		4		pF	8
$C_{I/O}$	Bidi. I/O Capacitance	Freq = 1 MHz @ 0 V		4	8	pF	8
I_{KLU}	I/O Latch-up Current	V < V_{SS}, V> V_{DD}	200			mA	
V_{ESD}	Electrostatic Protection	C=100 pF, R =1.5 KΩ	2000			V	
PD_G	Power Dissipation per gate			6		µW/Gate/MHz	9
PD_O	Power Dissipation per Output	C = 50 pF		1.5		mW/Output/MHz	9

Notes 1. Commercial 0 to 70°C, V_{DD} = 5 V ± 5%.
Industrial –40 to 85°C, V_{DD} = 5 V ± 5%.
Military –55 to 125 °C, V_{DD} = 5 V ± 10%.
2. Adherence to rules in Power Requirements section required.
3. Refer to the Design Manual for AC Testing Levels and Conditions
4. Buffers offered in 3, 6, 12, 16, 24, 48 mA TTL options. The 48mA buffer is rated for sink current only.
5. Buffers are available in 2, 4 and 8mA CMOS options.
6. If all outputs are CMOS then V_{OL} (Max) = 0.05V and I_O = + 1 µA
7. If all outputs are CMOS then V_{OH} (Min) = V_{DD}-0.05V and I_O = - 1 µA
8. Excluding Package.
9. Refer to section on Power Requirements.

APPENDIX - MACROCELL LIBRARY

Cell	Description	Gates
AND FUNCTIONS		
AN2	2 Input AND, Single Drive	4
AN2P	2 Input AND, Double Drive	5
AN3	3 Input AND, Single Drive	5
AN3P	3 Input AND, Double Drive	6
AN4	4 Input AND, Single Drive	6
AN4P	4 Input AND, Double Drive	7
NAND FUNCTIONS		
ND2	2 Input NAND, Single Drive	3
ND2P	2 Input NAND, Double Drive	5
ND3	3 Input NAND, Single Drive	4
ND3P	3 Input NAND, Double Drive	7
ND4	4 Input NAND, Single Drive	5
ND4P	4 Input NAND, Double Drive	10
ND5	5 Input NAND, Single Drive	6
ND5P	5 Input NAND, Double Drive	10
ND6	6 Input NAND, Single Drive	11
ND6P	6 Input NAND, Double Drive	12
ND8	8 Input NAND, Single Drive	13
ND8P	8 Input NAND, Double Drive	14
NOR FUNCTIONS		
NR2	2 Input NOR, Single Drive	3
NR2P	2 Input NOR, Double Drive	5
NR3	3 Input NOR, Single Drive	4
NR3P	3 Input NOR, Double Drive	7
NR4	4 Input NOR, Single Drive	5
NR4P	4 Input NOR, Double Drive	9
NR5	5 Input NOR, Single Drive	6
NR5P	5 Input NOR, Double Drive	10
NR6	6 Input NOR, Single Drive	11
NR6P	6 Input NOR, Double Drive	12
NR8	8 Input NOR, Single Drive	13
NR8P	8 Input NOR, Double Drive	14
OR FUNCTIONS		
OR2	2 Input OR, Single Drive	4
OR2P	2 Input OR, Double Drive	5
OR3	3 Input OR, Single Drive	5
OR3P	3 Input OR, Double Drive	6
OR4	4 Input OR, Single Drive	6
OR4P	4 Input OR, Double Drive	7

Cell	Description	Gates
AND-NOR FUNCTIONS		
AO1	2 Input AND into 3 Input NOR, $\overline{(AB+C+D)}$	5
AO2	Double 2 Input AND into 2 Input NOR, $\overline{(AB+CD)}$	5
AO2P	Double 2 Input AND into 2 Input NOR, Double Drive, (AB+CD)	9
AO5	Inverting 2 of 3 Majority Gate, $\overline{(AB+AC+BC)}$	6
AO6	2 Input AND into 2 Input NOR, $\overline{(AB+C)}$	4
AND-NOR FUNCTIONS		
AO2N	Double 2 Input AND into 2 Input NOR, Double Drive, (AB+CD)	
OR-NAND FUNCTIONS		
AO3	2 Input OR into 3 Input NAND, $\overline{((A+B)CD)}$	5
AO3P	2 Input OR into 3 Input NAND, Double Drive, $\overline{((A+B)CD)}$	9
AO4	Double 2 Input OR into 2 Input NAND, $\overline{((A+B)(C+D))}$	5
AO7	2 Input OR into 2 Input NAND, $\overline{((A+B)C)}$	4
AND-NOR-NOR FUNCTION		
EO1	2 Input AND + 2 Input NOR into 2 Input NOR, $\overline{(AB+not(C+D))}$	6
OR-NAND-NAND FUNCTIONS		
EON1	2 Input OR + 2 Input NAND into 2-Input NAND, $\overline{((A+B).not(CD))}$	6
EON1P	2 Input OR + 2 Input NAND into 2 Input NAND, Double Drive, $\overline{((A+B).not(CD))}$	10
ADDER FUNCTIONS		
FA1A	Full Adder	19
INVERTER FUNCTIONS		
B4I	Inverter, 4x(Z)	8
B4IP	Inverter, 8x(Z)	9
B5I	Inverter, 3x(Z)	4
B5IP	Inverter, 6x(Z)	7
IV	Inverter, 1x(Z)	2
IVA	Inverter, Double P Transistor, Single N Transistor	3
IVD	2x Drive Uncommitted Inverter Pair	4
IVP	Inverter, 2x(Z)	3
DUAL INVERTER FUNCTIONS		
B2I	Dual Inverters, 1x(Z1), 3x(Z2)	5
B2IP	Dual Inverters, 2x(Z1), 6x(Z2)	9
B3I	Dual Inverters, 2x(Z1), 2x(Z2)	5
B3IP	Dual Inverters, 4x(Z1), 4x(Z2)	9
IVDA	Dual Inverters, 1x(Y), 1x(Z)	3
IVDAP	Dual Inverters, 2x(Y), 2x(Z)	6
NON-INVERTING BUFFER FUNCTIONS		
BTREE	Internal Non-Inverting Buffer, Single In Phase Output	9

Cell	Description	Gates
EXCLUSIVE OR/NOR FUNCTIONS		
EN	2 Input Exclusive NOR, Single Drive	6
EN3	3 Input Exclusive NOR, Single Drive	13
EN3P	3 Input Exclusive NOR, Double Drive	14
ENP	2 Input Exclusive NOR, Double Drive	10
EO	2 Input Exclusive OR, Single Drive	6
EO3	3 Input Exclusive OR, Single Drive	13
EO3P	3 Input Exclusive OR, Double Drive	14
EOP	2 Input Exclusive OR, Double Drive	10
INTERNAL TRISTATE FUNCTIONS		
BTS4	Internal Tristate Buffer, Positive Enable, Single Drive	5
BTS4P	Internal Tristate Buffer, Positive Enable, Double Drive	7
BTS5	Internal Tristate Inverting Buffer, Positive Enable, Single Drive	4
BTS5P	Internal Tristate Inverting Buffer, Positive Enable, Double Drive	7
D FLIP-FLOP FUNCTIONS		
FD1	D Flip-Flop, Buffered Outputs	14
FD1P	D Flip-Flop, Double Buffered Outputs	16
FD1S	D Flip-Flop with Scan Input, Buffered Outputs	21
FD2	D Flip-Flop with Clear, Buffered Outputs	20
FD2P	D Flip-Flop with Clear, Double Buffered Outputs	22
FD2S	D Flip-Flop with Scan Input with Clear, Buffered Outputs	22
FD2TS	D Flip-Flop with Added Tristate Ouput	20
FD3	D Flip-Flop with Clear and Preset, Buffered Outputs	24
FD3P	D Flip-Flop with Clear and Preset, Double Buffered Outputs	25
FD3S	D Flip-Flop with Scan Input, Clear and Preset, Buffered Outputs	26
FD4	D Flip-Flop with Preset, Buffered Outputs	18
FD4P	D Flip-Flop with Preset, Double Buffered Outputs	20
FD4S	D Flip-Flop with Scan Input, Preset, Buffered Outputs	23
J K FLIP-FLOP FUNCTIONS		
FJK1	JK Flip-Flop, Buffered Outputs	20
FJK1P	JK Flip-Flop, Double Buffered Outputs	21
FJK1S	JK Flip-Flop with Scan Input, Buffered Output	26
FJK2	JK Flip-Flop with Clear, Buffered Outputs	27
FJK2P	JK Flip-Flop with Clear, Double Buffered Outputs	25
FJK2S	JK Flip-Flop with Scan Input, Clear, Buffered Outputs	28
FJK3	JK Flip-Flop with Clear and Preset, Buffered Outputs	29
FJK3P	JK Flip-Flop with Clear and Preset, Double Buffered Output	31
FJK3S	JK Flip-Flop with Scan Input, Clear and Preset, Buffered Outputs	32

Cell	Description	Gates
LATCH FUNCTIONS		
LD1	D-Latch, Active High Clock, Buffered Outputs	10
LD1P	D-Latch, Active High Clock, Double Buffered Outputs	12
LD2	D-Latch, Active Low Clock, Buffered Outputs	10
LD2P	D-Latch, Active Low Clock, Double Buffered Outputs	12
LD3	D-Latch, Active High Clock, Active Low Clear, Buffered Outputs	12
LD3P	D-Latch, Active High Clock, Active Low Clear, Double Buffered Outputs	13
LD4	D-Latch, Active Low Clock, Active Low Clear, Buffered Outputs	12
LD4P	D-Latch, Active Low Clock, Active Low Clear, Double Buffered Outputs	13
LS1	D-Latch with Scan Test Inputs, Dual Active High Clocks, Buffered Out.	17
LS2	LS1 D-Latch into LD1 D-Latch, Active High Clocks, Buffered Outputs	26
LSR1	SR Latch with Clear/Set, Separate Inputs, (Cross Coupled AO3 Macros)	9
LSR2	SR Latch with Clear/Set, Common Gated Inputs, (Cross Coupled AO3 Macros)	9
RAM1	Gated D-Latch with Added Tristate Output	11
MULTIPLEXER FUNCTIONS		
MUX21L	2:1 Multiplexer, 1 Phase Select, Unbuffered Inputs, Inverting Buffered Output	6
MUX21LA	2:1 Multiplexer, 2 Phase Select, Unbuffered Inputs, Inverting Buffered Output	5
MUX21LP	2:1 Multiplexer, 1 Phase Select, Unbuffered Inputs, Inverting Double Buffered Output	7
MUX41	4:1 Multiplexer, Buffered Inputs, 2 Select Lines, Buffered Output	17
MUX41L	4:1 Multiplexer, Buffered Inputs, 2 Select Lines, Inverting Buffered Out.	19
MUX41P	4:1 Multiplexer, Buffered Inputs, 2 Select Lines, Double Drive Buffered Output	18
MUX81	8:1 Multiplexer, Buffered Inputs, 3 Select Lines, Buffered Output	34
MUX81H	8:1 Multiplexer, Buffered Inputs, 3 Select Lines, Buffered Output	34
MUX81P	8:1 Multiplexer, Buffered Inputs, 3 Select Lines, Double Buffered Out.	35

Cell	Description	Standard Units
CMOS OUTPUT BUFFER		
B2CR	CMOS Output Buffer, 2mA, Slew Rate Control	1
B4CR	CMOS Output Buffer, 4mA, Slew Rate Control	2
B8CR	CMOS Output Buffer, 8mA, Slew Rate Control	4
TTL OUTPUT BUFFERS		
B2R	TTL Output Buffer, 2mA, with Slew Rate Control	2
B4	TTL Output Buffer, 4mA	8
B4R	TTL Output Buffer, 4mA, with Slew Rate Control	4
B4ROD	TTL Open Drain Output Buffer, 4mA, with Slew Rate Control	4
B8	TTL Output Buffer, 8mA	16
B8R	TTL Output Buffer, 8mA, with Slew Rate Control	8
B8ROD	TTL Open Drain Output Buffer, 8mA, with Slew Rate Control	8
CMOS BIDIRECTIONAL BUFFER		
BD2C	Bidirectional CMOS I/O Buffer, 2mA	2
BD2CR	Bidirectional CMOS I/O Buffer, 2mA, with Slew Rate Control	1
BD2CRU	Bidirectional CMOS I/O Buffer, Active Pull Up, 2mA, Slew Rate Control	1
BD2SCR	Bidirectional CMOS I/O Buffer, Schmitt trigger Input, 2mA, Slew Rate Control	1
BD2SCRU	Bidirectional CMOS I/O Buffer, Schmitt trigger Input, Active Pull Up, 2mA, with Slew Rate Control	1
BD4C	Bidirectional CMOS I/O Buffer, 4mA	4
BD4CR	Bidirectional CMOS I/O Buffer, 4mA, with Slew Rate Control	2
BD4CRU	Bidirectional CMOS I/O Buffer, Active Pull Up, 4mA, with Slew Rate Control,	2
BD4SCR	Bidirectional CMOS I/O Buffer, Schmitt Trigger Input, 4mA, with Slew Rate Control,	2
BD4SCROD	Bidirectional CMOS I/O Buffer, Schmitt Trigger Input, Open Drain Output, 4mA, with Slew Rate Control,	2
BD4SCRU	Bidirectional CMOS I/O Buffer, Active Pull Up, Schmitt Trigger Input, 4mA, Slew Rate Control,	2
BD8SCR	Bidirectional CMOS I/O Buffer, Schmitt Trigger Input, 8mA, Slew Rate Control,	4
BD8SCRU	Bidirectional CMOS I/O Buffer, Active Pull Up, Schmitt Trigger Input, 8mA, Slew Rate Control,	4
TTL BIDIRECTIONAL BUFFERS		
BD2STR	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, 2 mA , with Slew Rate Control	2
BD2STRU	Bidirectional TTL I/O Buffer, Active pull Up, Schmitt Trigger Input, 2 mA, with Slew Rate Control	2
BD2TR	Bidirectional TTL I/O Buffer, 2 mA, with Slew Rate Control	2
BD2TRU	Bidirectional TTL I/O Buffer, Active Pull Up,with Slew Rate Control	2

Cell	Description	Standard Units
BD4STR	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, 4mA, with Slew Rate Control	4
BD4STROD	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, Open Drain Output, 4mA, with Slew Rate Control	4
BD4STRU	Bidirectional TTL I/O Buffer, Active Pull-Up, Schmitt Trigger Input, 4mA, with Slew Rate Control	4
BD4T	Bidirectional TTL I/O Buffer, 4mA	8
BD4TR	Bidirectional TTL I/O Buffer, 4mA, with Slew Rate Control	4
BD4TRU	Bidirectional TTL I/O Buffer, Active Pull-Up, 4mA, with Slew Rate Control	4
BD8STR	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, 8mA, with Slew Rate Control	8
BD8STRD	Bidirectional TTL I/O Buffer, Active Pull Down, Schmitt Trigger Input, 8mA, with Slew Rate Control	8
BD8STROD	Bidirectional TTL I/O Buffer, Schmitt Trigger Input, Open drain Output, 8mA, with Slew Rate Control	8
BD8STRU	Bidirectional TTL I/O Buffer, Active Pull-Up, Schmitt Trigger Input, 8mA, with Slew Rate Control	8
CMOS TRISTATE OUTPUT BUFFERS		
BT2CR	CMOS Tristate Output Buffer 2 mA with Slew Rate Control	1
BT2CRU	CMOS Tristate Output Buffer, Active Pull Up, 2mA with Slew Rate Control	1
BT4CR	CMOS Tristate Output Buffer, 4mA with Slew Rate Control	2
BT4CRU	CMOS Tristate Output Buffer, Active Pull-Up, 4mA, with Slew Rate Control	2
BT8CR	CMOS Tristate Output Buffer, 8mA with Slew Rate Control	4
BT8CRU	CMOS Tristate Output Buffer, Active Pull Up, 8mA with Slew Rate Control	4
TTL TRISTATE OUTPUT BUFFERS		
BT2R	TTL Tristate Output Buffer, 4mA, with Slew Rate Control	2
BT2RU	TTL Tristate Output Buffer, Active Pull-Up, 4mA, with Slew Rate Control	2
BT4	TTL Tristate Output Buffer, 2mA,	8
BT4OD	TTL Tristate Open Drain Output Buffer, 4mA	8
BT4R	TTL Tristate Output Buffer, 4mA, with Slew Rate Control	4
BT4RU	TTL Tristate Output Buffer, Active Pull-Up, 4mA, with Slew Rate Control	4
BT8	TTL Tristate Output Buffer, 8mA	16
BT8OD	TTL Tristate Open Drain Output Buffer, 8mA	16
BT8R	TTL Tristate Output Buffer, 8mA, with Slew Rate Control	8
BT8RU	TTL Tristate Output Buffer, Active Pull-Up, 8mA, with Slew Rate Control	8
TTL BUS DRIVER OUTPUT BUFFER		
BU6R	TTL Bus Driver Output Buffer, 6mA with Slew Rate Control	6
BU12R	TTL Bus Driver Output Buffer, 12mA with Slew Rate Control	12

Cell	Description	Standard Units
BU18R	TTL Bus Driver Output Buffer, 18mA with Slew Rate Control	18
BU24R	TTL Bus Driver Output Buffer, 24mA with Slew Rate Control	24
TTL BIDIRECTIONAL BUFFER WITH TRISTATE BUS DRIVER OUTPUT		
BUD6STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 6mA, with Slew Rate Control	6
BUD6STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 6mA, (S = 5V)	12
BUD6STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 6mA, (S = 0V)	6
BUD12STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 12mA, with Slew Rate Control	12
BUD12STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 12mA, (S = 5V)	24
BUD12STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 12mA, (S = 0V)	12
BUD18STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 18mA, with Slew Rate Control	18
BUD18STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 18mA, (S = 5V)	36
BUD18STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 18mA, (S = 0V)	18
BUD24STR	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 24mA, with Slew Rate Control	24
BUD24STVN	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 24mA, (S = 5V)	48
BUD24STVS	TTL Bidirectional Buffer, Schmitt Trigger Input, Tristate Bus Driver Output 24mA, (S = 0V)	24
TTL TRISTATE BUS DRIVER OUTPUT BUFFER		
BUT6R	TTL Tristate Bus Driver Output Buffer, 6mA with Slew Rate Control	6
BUT12R	TTL Tristate Bus Driver Output Buffer, 12mA with Slew Rate Control	12
BUT18R	TTL Tristate Bus Driver Output Buffer, 18mA with Slew Rate Control	18
BUT24R	TTL Tristate Bus Driver Output Buffer, 24mA with Slew Rate Control	24
CMOS INPUT BUFFERS		
IBUF	CMOS Input Buffer	–
IBUFD	CMOS Input Buffer with Active Pull-Down	–
IBUFN	Inverting CMOS Input Buffer	–
IBUFU	CMOS Input Buffer with Active Pull-Up	–
TTL INPUT BUFFERS		
TLCHT	TTL Input Buffer	–
TLCHTD	TTL Input Buffer, Active Pull-Down	–

Cell	Description	Standard Units
TLCHTN	TTL Input Buffer	–
TLCHTU	TTL Input Buffer, Active Pull-Up	–
SCHMITT INPUT BUFFERS		
SCHMITC	CMOS Schmitt Trigger Input Buffer	–
SCHMITCD	CMOS Schmitt Trigger Input Buffer, Active Pull-Down	–
SCHMITCN	Inverting CMOS Schmitt Trigger Input Buffer	–
SCHMITCU	CMOS Schmitt Trigger Input Buffer, Active Pull-Up	–
SCHMITT	TTL Schmitt Trigger Input Buffer	–
SCHMITTD	TTL Schmitt Trigger Input Buffer, Active Pull-Down	–
SCHMITTN	Inverting TTL Schmitt Trigger Input Buffer	–
SCHMITTU	TTL Schmitt Trigger Input Buffer, Active Pull-Up	–